

# AMD Opteron™ Processor Product Data Sheet



- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3\*, MMX™, 3DNow!™ technology and legacy x86 instructions
  - \*SSE3 supported by Rev E and later
  - Runs existing operating systems and drivers
  - Local APIC on the chip
- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight additional 64-bit integer registers (16 total)
  - Eight additional 128-bit SSE/SSE2/SSE3 registers (16 total)
- **Multi-Core Architecture**
  - Single-core or dual-core options
  - Discrete L1 and L2 cache structures for each core
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
  - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
  - With advanced branch prediction
- **1024-Kbyte (1-Mbyte) 16-Way Associative ECC-Protected L2 Cache**
  - Exclusive cache architecture—storage in addition to L1 caches
  - Up to 1 Mbyte per L2 cache
- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
  - Multiple low-power states
  - System Management Mode (SMM)
  - ACPI compliant, including support for processor performance states

## 940-Pin Package Specific Features

- **Refer to the *AMD Functional Data Sheet, 940-Pin Package*, order# 31412, for functional, electrical, and mechanical details of 940-pin processors.**
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-Like differential, unidirectional
  - DDR SDRAM: SSTL\_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
  - 940-pin lidded ceramic or organic micro PGA
  - 1.27-mm pin pitch
  - 31 x 31 row pin array
  - 40 mm x 40 mm ceramic or organic substrate
  - Ceramic or organic C4 die attach
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz (200 MHz supported by Rev C0 and later)
  - Supports up to eight registered DIMMs
  - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
  - Three links, 16-bits in each direction, each supports up to 2000 MT/s or 4.0 GB/s in each direction (2000MT/s supported by Rev E and later)
  - Each link on uniprocessor (UP) models supports connections to I/O devices.
  - Each link on dual-processor (DP) models supports connections to I/O devices, and any one of the three available links may connect to another DP or MP processor.
  - Each link on multiprocessor (MP) models supports connections to I/O devices or other DP or MP processors.

Publication #	<b>23932</b>	Revision:	<b>3.23</b>
Issue Date:	<b>March 2007</b>		

## 939-Pin Package Specific Features

- Refer to the *AMD Functional Data Sheet, 939-Pin Package, order# 31411*, for functional, electrical, and mechanical details of 939-pin package processors.
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-Like differential, unidirectional
  - DDR SDRAM: SSTL\_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
  - 939-pin lidded micro PGA
  - 1.27-mm pin pitch
  - 31 x 31 row pin array
  - 40 mm x 40 mm organic substrate
  - Organic C4 die attach
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz
  - Supports up to four unbuffered DIMMs
  - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

## Socket AM2 Processor Specific Features

- Refer to the *Socket AM2 Processor Functional Data Sheet, order# 31117*, for functional and mechanical details of socket AM2 processors.
- Refer to the *AMD NPT 0Fh Family Processor Electrical Data Sheet, order# 31119*, for electrical details of socket AM2 processors.
- **Electrical Interfaces**
  - HyperTransport™ Technology: LVDS-like differential, unidirectional
  - DDR2 SDRAM: SSTL\_1.8 per JEDEC specification
  - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications
- **Packaging**
  - Lidded micro PGA
  - 31 x 31 grid array
  - 1.27-mm pin pitch
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR2 SDRAM controller operating at up to 333 MHz
  - Supports up to four unbuffered DIMMs
  - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

## Socket F (1207) Processor Specific Features

- **Refer to the *Socket F (1207) Processor Functional Data Sheet*, order# 31118 for functional and mechanical details of socket F (1207) processors.**
- **Refer to the *AMD NPT 0Fh Family Processor Electrical Data Sheet*, order# 31119 for electrical details of socket F (1207) processors.**
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-Like differential, unidirectional
  - DDR2 SDRAM: SSTL\_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications
- **Packaging**
  - Lidded Land Grid Array package
  - 35 x 35 grid array
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR2 SDRAM at up to 333 MHz
  - Supports up to eight registered DIMMs
  - ECC checking with double-bit detect and single-bit correct
  - On-line spare feature provides single-rank DRAM redundancy
- **HyperTransport™ Technology to I/O Devices**
  - Three links, 16-bits in each direction, each supports up to 2000 MT/s or 4.0 GB/s in each direction (2000MT/s supported by Rev E and later)
  - Each link on uniprocessor (UP) models supports connections to I/O devices.
  - Each link on dual-processor (DP) models supports connections to I/O devices, and any one of the three available links may connect to another DP or MP processor.
  - Each link on multiprocessor (MP) models supports connections to I/O devices or other DP or MP processors.

## Revision History

Date	Revision	Description
March 2007	3.23	Public release. <ul style="list-style-type: none"> <li>Corrected typo.</li> <li>Updated reference to <i>Socket F (1207) Processor Functional Data Sheet</i>.</li> </ul>
August 2006	3.19	Public release. Added RoHS compliance statement to Socket AM2 and Socket F (1207) specific features sections.
July 2006	3.17	Public release.
June 2005	3.13	Formatting changes. Updated with Rev E features.

---

© 2005 – 2007 Advanced Micro Devices, Inc. All rights reserved.

The contents of this document are provided in connection with Advanced Micro Devices, Inc. (“AMD”) products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. The information contained herein may be of a preliminary or advance nature and is subject to change without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD’s Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD’s products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD’s product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

---

### Trademarks

AMD, the AMD Arrow logo, AMD Opteron, and combinations thereof, and 3DNow! are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

MMX is a trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.